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Authors	Nidor Huang

Quick Start Guide

for

SOM-352 Family

Product Variants

Model	Description
SOM-352	V2X mPCIe System-On-Module, 0A1
SOM-352ED	V2X mPCIe System-On-Module, V2Xcast® - ITS-G5 stack, Europe, 0A1
SOM-352UC	V2X mPCIe System-On-Module, V2Xcast® - C-V2X stack, USA, 0A1
SOM-352UD	V2X mPCIe System-On-Module, V2Xcast® - WAVE stack, USA, 0A1

Reviewers

Department	Name	Acceptance Date	Note
PD	Nidor Huang	2023/07/10	
RD	P.C. Kang	2023/07/10	

Modification History

Revision	Date	Originator	Comment
0.1	2021/08/19	Nidor Huang	Creating document
0.2	2021/10/13	Nidor Huang	Adding product variants Adding limited warranty policies, safety guidelines and product appearance Adding reset and 1PPS guidelines Adding software settings Rearranging chapter order Changing document type from HDG to QSG
0.3	2021/11/15	Nidor Huang	Updating J1.1 description Adding antenna cable extraction instructions Adding troubleshooting
0.4	2022/04/15	Nidor Huang	Adding GNSS antenna detection mechanism
0.5	2022/07/08	Nidor Huang	Modifying antenna cable extraction instructions Adding tamper backup power description

Revision	Date	Originator	Comment
0.6	2022/12/30	Nidor Huang	Changing model variants to SOM-352 family Updating functional block diagram Adding mPCIe Pin 46 BOOTSTRP Adding 1PPS pin BSP description
0.7	2023/03/03	Nidor Huang	Adding V2X antenna detection function Updating Unex BSP interface settings Updating BOOTSTRP timing description Updating product photos
0.8	2023/03/08	Nidor Huang	Updating Unex logo Adding GNSS reset in Unex BSP interface settings
0.9	2023/05/10	Nidor Huang	Changing Ethernet over USB protocol to RNDIS
1.0	2023/07/10	Nidor Huang	Updating functional block diagram Removing EC series from product variants

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Objective

The purpose of this document is to provide necessary information to help setup and installation of SOM-352 series products. To provide for safe installation and operation of the equipment, read the safety guidelines at the beginning of this manual and follow the procedures outlined in the following chapters before connecting power to SOM-352. Keep this operating manual handy and distribute to all users, technicians and maintenance personnel for reference.

1. Reference

- PCI Express Mini Card Electromechanical Specification 2.0/2.1
- I-PEX MHF Micro RF coax connector product series catalog
- HIM-10002-06EN: I-PEX MHF I Connector Instruction Manual
- Unex SOM-352 datasheet
- SOM-352 drawing 51-00009-00
- Unex's documentation (in Unex's software release package)

2. Limited Warranty Policy

Unex Technology Corporation selling the product warrants that commencing from the date of shipment to customer and continuing for a period of twelve (12) months. This limited warranty extends only to the original customer of the product. Customer's sole and exclusive remedy and the entire liability of Unex under this limited warranty will be, at Unex's option, return for repair to Unex's repair center with freight and insurance prepaid or shipment of a replacement within the warranty period or a refund of the purchase price if the hardware is returned to Unex. Unex's obligations hereunder are conditioned upon the return of affected hardware in accordance with Unex's service center's then-current Return Material Authorization (RMA) procedures.

This warranty does not cover:

- Products found to be defective after the warranty period has expired.
- Products subjected to misuse or abuse, whether by accident or other causes. Such product conditions will be determined by Unex at its sole and unfettered discretion.
- Products damaged due to a natural disaster, including but not limited to

lightning, flooding, earthquake, or fire.

- Software products.
- Products dismantled or opened by unauthorized persons. Please contact a representative of Unex if you need advanced technical support.
- Products with an altered and/or damaged serial number.
- Loss of data or software.
- Products that have been updated, reworked, or improperly tested by the Customer, or by a third party at the request of the Customer.
- Customized and original design manufacturer (ODM) products. The warranty terms for customized and ODM products should be defined in the contract that governs the project.

3. Safety Guidelines

- Keep working area clean and dry while assembling/installing.
- When operating under extreme temperature conditions, environmental control measures (e.g., heating, cooling) should be considered.
- Make sure every accessory has been fastened, including the V2X antenna cables, GNSS antenna cable, and the mPCIe socket latch/screws.

4. Product Appearance

The photos shown in this document may seem different from actual product. However, the differences do not affect actual functionalities.

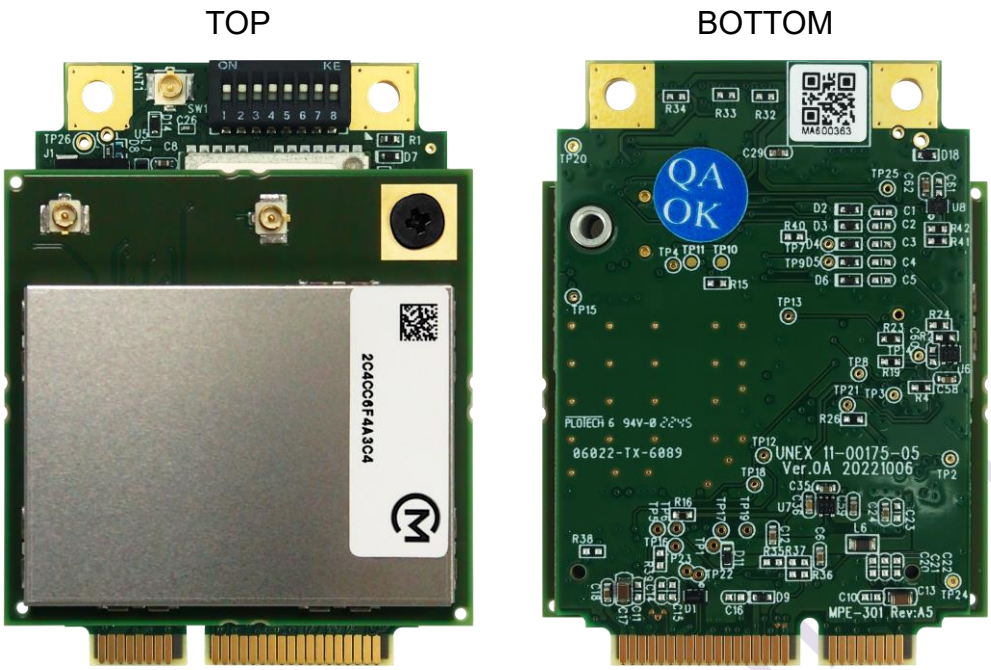

Figure 1: SOM-352 series appearance

5. Functional Block Diagram

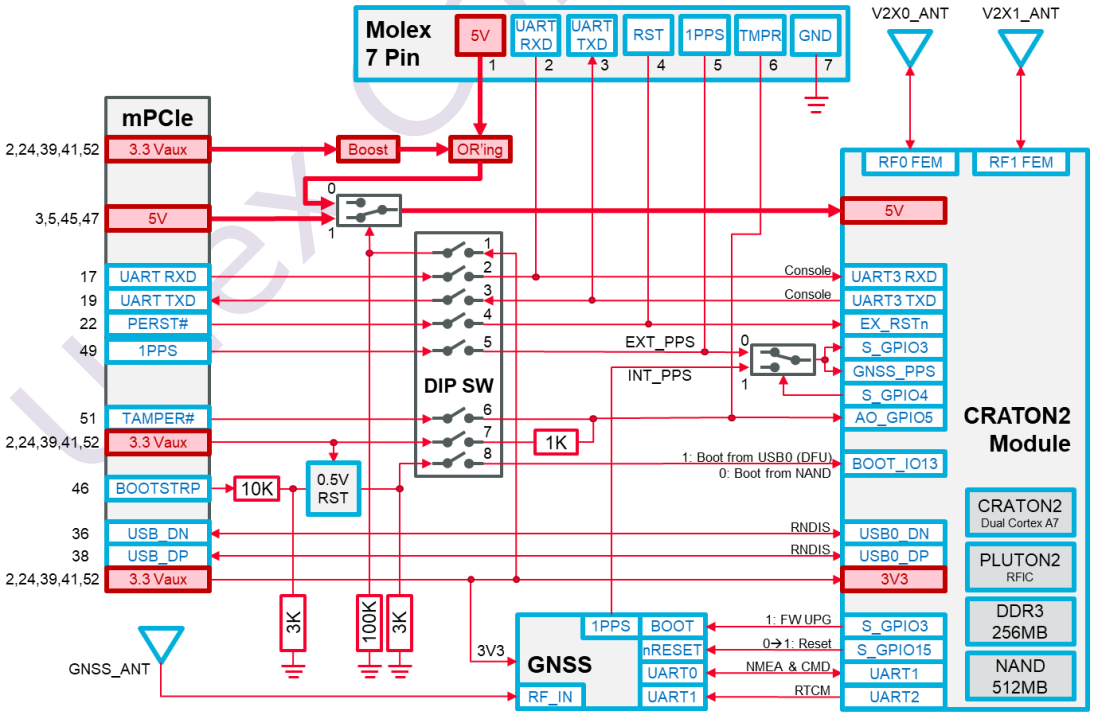

Figure 2: Functional block diagram

6. Electrical Characteristics

6.1. Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted).

Table 1. Absolute maximum ratings

Parameters	Conditions	Min.	Max.	Unit
Storage Temperature	-	-40	105	°C
Supply Voltage	mPCIe 5V	-0.3	6.0	V
	mPCIe 3.3 Vaux	-0.3	3.9	V
V2X maximum input level	-	-	10	dBm
GNSS maximum input level	-	-	-10	dBm

Note:
(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltages are with respect to network GND.

6.2. Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted).

Table 2. Recommended operating conditions

Parameters	Conditions	Min.	Typ.	Max.	Unit
Ta (Ambient operating temperature)	Free-air temp.	-40	25	85	°C
Supply voltage	mPCIe 5V	4.8	5.0	5.2	V
	mPCIe 3.3 Vaux	3.0	3.3	3.6	V
VIL (Input low level voltage)	mPCIe 5V = 5.0V	-0.3	-	0.8	V
VIH (Input high level voltage)	mPCIe 5V = 5.0V	2.0	-	3.6	V
	TAMPER#	2.0	-	3.3 Vaux +0.3	V
RPU (Equivalent pull-up)	1PPS/UART *1	32	50	60	kΩ
	PERST#/EX_RSTn	1.8	2.1	2.3	kΩ
	TAMPER# *2	0.9	1.0	1.1	kΩ
RPD (Equivalent pull-down)	TAMPER# *3	32	50	60	kΩ
VOL (Output low level voltage)	IOL= 4mA *4	-	-	0.4	V
VOH (Output high level voltage)	IOH= 4mA *5	2.9	-	-	V

Parameters	Conditions	Min.	Typ.	Max.	Unit
mPCIe 1PPS (P49) tolerance	Accuracy/Bias	-100	-	100	ns
	Precision/Jitter	-30	-	30	ns
	Pulse width	15	-	-	ns
V2X sensitivity	PER ≤ 10%	-92	-	-	dBm
	PER ≤ 10%, -40 - +85 °C	-82	-	-	dBm
V2X maximum input level	PER ≤ 10%	-	-	-30	dBm
V2X adjacent channel rejection	-	13	-	-	dB
V2X non-adjacent channel rejection	-	29	-	-	dB
V2X output power	Spectrum mask Class C	-	-	20	dBm
GNSS sensitivity (C/N_0)	Acquisition	22	30	45	dB-Hz
GNSS antenna bias	I_{ANT} ≤ 20mA	3.0	-	3.3	V
GNSS antenna detection current	I_{ANT} *6	12	-	58	mA
GNSS maximum total external gain	Gain/loss combined	-	-	24	dB

Note:
*1: UART = UART_RX (mPCIe P17) / UART_TX (mPCIe P19) / RXD (Molex P2) / TXD (Molex P3)
*2: TRIGGER_SW (SW1.7) = ON
*3: TRIGGER_SW (SW1.7) = OFF
*4: IOL = Low level output current (UART_TX)
*5: IOH = High level output current (UART_TX)
*6: I_{ANT} under Min. = OPEN; I_{ANT} over Max. = SHORT; I_{ANT} between Min/Max. = NORMAL.

6.3. Power Consumption

SOM-352 can be powered in three different ways: dual voltage (5V/3.3V), external cable (5V/3.3V), and single voltage (3.3V). The data listed in table 3, 4, and 5 serve only as a reference for system integrators. The actual conditions will vary depending on firmware version and user applications.

Table 3. Dual voltage power consumption

Condition			Power Consumption (A)		
Temp.	**Power Source**	**Voltage (V)**	**Low** *1	**Typical** *2	**High** *3
25°C	5V *4	5	0.34	0.40	2.0
	3.3 Vaux *5	3.3	0.100	0.105	0.110
85°C	5V *4	5	0.38	0.44	2.0
	3.3 Vaux *5	3.3	0.105	0.110	0.115

Condition	Power Consumption (A)

Note:
*1: CPU idle and V2X stack loaded.
*2: CPU 50% and V2X transmitting 400 bytes at 20dBm every 100ms.
*3: Hardware upper limit.
*4: From mini PCIe 5V (pin 3, 5, 45, 47)
*5: From mini PCIe 3.3 Vaux (pin 2, 24, 39, 41, 52)

Table 4. External cable power consumption

Condition			Power Consumption (A)		
Temp.	**Power Source**	**Voltage (V)**	**Low** *1	**Typical** *2	**High** *3
25°C	5V *4	5	0.34	0.40	2.0
	3.3 Vaux *5	3.3	0.100	0.105	0.110
85°C	5V *4	5	0.38	0.44	2.0
	3.3 Vaux *5	3.3	0.105	0.110	0.115

Note:
*1: CPU idle and V2X stack loaded.
*2: CPU 50% and V2X transmitting 400 bytes at 20dBm every 100ms.
*3: Hardware upper limit.
*4: From Molex 7 pin connector (pin 1)
*5: From mini PCIe 3.3 Vaux (pin 2, 24, 39, 41, 52)

Table 5. Single voltage power consumption

Condition			Power Consumption (A)		
Temp.	**Power Source**	**Voltage (V)**	**Low** *1	**Typical** *2	**High** *3
25°C	3.3 Vaux *4	3.3	0.60	0.70	3.0
85°C	3.3 Vaux *4	3.3	0.70	0.77	3.0

Note:
*1: CPU idle and V2X stack loaded.
*2: CPU 50% and V2X transmitting 400 bytes at 20dBm every 100ms.
*3: Hardware upper limit.
*4: From mini PCIe 3.3 Vaux (pin 2, 24, 39, 41, 52)

7. I/O Interfaces

7.1. Antenna Connectors

The SOM-352 mPCIe module is provided with three 50 Ω RF connectors (see FIGURE 3: ANTENNA CONNECTORS):

- two V2X antennas

- one GNSS antenna

Receptacle connectors are *I-PEX MHF I 20279-001E-03*. For more information about mating plug connectors, visit the website https://www.i-pex.com/product/mhf-I or for more detail.

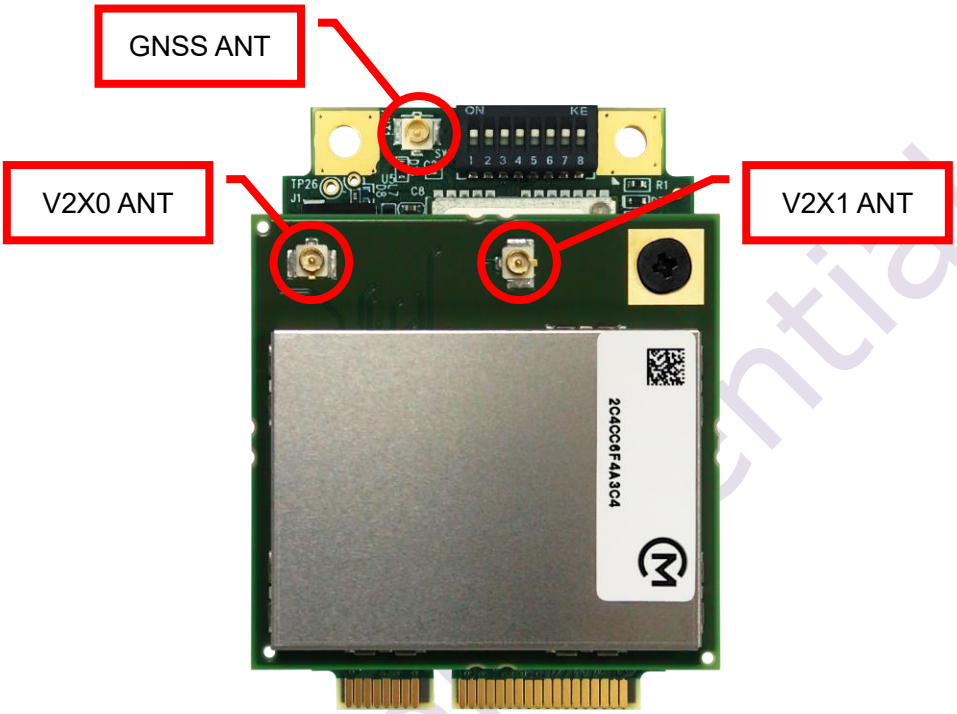

Figure 3: Antenna connectors

The antenna connection is one of the most important aspects in the full product design as it strongly affects the RF performance. Connecting cables between the module and the antenna must have 50 Ω impedance. If the impedance of the module is mismatched, RF performance will be reduced significantly.

Please be careful when extracting the antenna cables from a SOM-352 module. Extracting the connector by pulling the cable may cause damage on the antenna plug assembly. It is recommended to extract the cable using a proper extraction tool suggested by the cable plug manufacturer. For I-PEX plugs please use *I-PEX 90192-001 or 90224-001*.

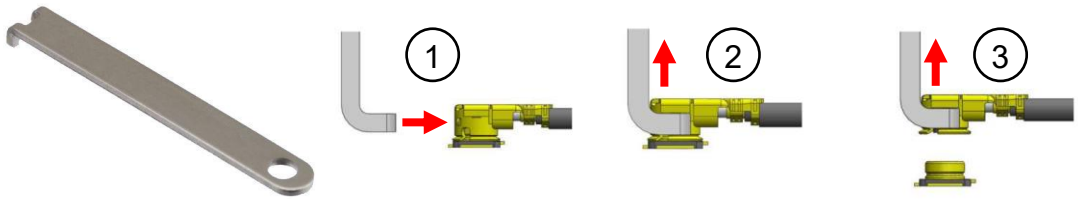

Figure 4: Antenna cable extraction tool

Caution 	1 Always use only the extraction tool recommended by the plug manufacturer of your choice. It is possible to cause severe damage on the receptacle if a third-party extraction tool is used. For example, using an I-PEX tool on a HIROSE plug has been known to lead to connector damages. 2 It is very important to keep the extraction tool at a vertical position at all time, and apply only vertical pulling force on the tool. Applying a non-vertical force or using the tool in a crowbar style will damage not only the antenna connector but also other components in proximity. 3 Please follow HIM-10002-06EN for more detailed instructions.

7.1.1. 5.9GHz V2X

The V2X antenna ports has a built-in antenna detection function (see TABLE 6). This detection mechanism only works with Unex V2X antennas EX-55 or EX-53 antennas. EX-55/EX-53 antennas are not included in SOM-352 product package and can be purchased separately.

Table 6: V2X antenna status

Antenna Status	Value	Command
OPEN	616-1023	V2X0: cat /sys/bus/iio/devices/iio\:device0/in_voltage4_raw V2X1: cat /sys/bus/iio/devices/iio\:device0/in_voltage5_raw
NORMAL	410-615	
SHORT	0-409	

EX-55

Gain:	5dBi
Radiation Pattern:	Omni-directional
Application:	Indoor/OBU
Connector:	FAKRA-Z

EX-53

Gain:	7.6dBi
Radiation Pattern:	Omni-directional
Application:	Outdoor/RSU
Connector:	Type N

Figure 5: V2X antennas EX-55/EX-53

7.1.2. GNSS

For stable fix acquisition, at least 4 satellites with enough signal strength (C/N_0 value above 30 dB-Hz) are required. If the signal strength goes below 30 dB-Hz, the fix will become unstable.

7.1.2.1. GNSS Antenna Detection

The antenna detection mechanism is a 2-step process: First check the signal strength. If the signal strength drops to zero, then check the antenna status flag.

When all the C/N_0 values becomes null, it means that the GNSS antenna or its cable may either become detached or damaged. The GNSS antenna port has a built-in antenna detection function. The detection mechanism is based on the current consumption of an active antenna (I_{ANT}). If the active antenna consumes less current than 12 mA, then it is considered as the OPEN status; if the antenna consumes more than 58 mA, then it is considered as the SHORT status. Anything between 12-58 mA is considered as the NORMAL status.

The GNSS 3.3V antenna bias will be continuously supplied in OPEN/NORMAL status. Once the SHORT status is triggered, the SHORT flag will persist, and the 3.3V bias will be turned off until the reset of the GNSS module. After the reset of the GNSS module, the detection process will start all over again.

It is possible for a good active antenna to be reported OPEN because it consumes less current than 12 mA, or a good passive antenna to be considered SHORT because it is DC shorted (e.g., a slot antenna). However, as long as there are more than 4 satellites with enough signal strength (C/N_0 value above 30 dB-Hz), the GNSS is in good state.

The antenna status flag is reported in a proprietary NMEA message:

```
$PSTMANTENNASTATUS,<status>*<checksum><cr><lf>
```

where `<status>` can be:

- 0 - The antenna current is in the normal range (NORMAL)
- 1 - The antenna current is below the normal range (OPEN)
- 2 - The antenna current is above the normal range (SHORT)

Table 7: GNSS antenna status

Antenna Status	Current Consumption (mA)	3.3V bias	NMEA Sentence
OPEN	< 12	ON	$PSTMANTENNASTATUS,1*4C
NORMAL	between 12- 58	ON	$PSTMANTENNASTATUS,0*4D
SHORT	> 58	Turned OFF once triggered	$PSTMANTENNASTATUS,2*4F

7.2. Mini PCIe Card Pinout

There are 3 groups of pins in the SOM-352 mPCIe pinout:

4 Group 1: Proprietary pins, originally marked as reserved in mPCIe standard interface

5 Group 2: Standard mPCIe pins used by SOM-352, including 3.3 Vaux, ground, PERST#, and USB data lines

6 Group 3: Standard mPCIe pins but not used in SOM-352, marked NC

SOM-352 only needs group1 and group2 pins for normal operation. For maximize compatibility with existing mPCIe modules on the market, it is suggested to connect all three groups of pins to the mPCIe connector.

Please note that the I/O directions listed here are on the SOM-352 side. For designing a system board mPCIe interface, the input and output direction must be reversed.

Table 8: SOM-352 mini PCIe row 0 pinout

Pin	Symbol	Type	Level (V)	Description	Note
1	NC	-	-	Not connected	
3	5V	P	5	5V/2A power input	Proprietary
5	5V	P	5	5V/2A power input	Proprietary
7	NC	-	-	Not connected	
9	GND	G	-	Ground	
11	NC	-	-	Not connected	
13	NC	-	-	Not connected	
15	GND	G	-	Ground	
-	KEY	-	-	Mechanical key	
17	UART_RX	I (PU)	3.3	UART received data	Proprietary
19	UART_TX	O (PU)	3.3	UART transmitted data	Proprietary
21	GND	G	-	Ground	
23	NC	-	-	Not connected	
25	NC	-	-	Not connected	
27	GND	G	-	Ground	
29	GND	G	-	Ground	
31	NC	-	-	Not connected	
33	NC	-	-	Not connected	

Pin	Symbol	Type	Level (V)	Description	Note
35	GND	G	-	Ground	
37	GND	G	-	Ground	
39	3.3 Vaux	P	3.3	Powered by 5V: 115mA (max) Powered by 3.3 Vaux: 3000mA (max)	
41	3.3 Vaux	P	3.3	Powered by 5V: 115mA (max) Powered by 3.3 Vaux: 3000mA (max)	
43	GND	G	-	Ground	
45	5V	P	5	5V/2A power input	Proprietary
47	5V	P	5	5V/2A power input	Proprietary
49	1PPS	I (PU)	3.3	GNSS 1PPS input (active HIGH)	Proprietary
51	TAMPER#	I (PU/PD)	3.3	Tamper detection (active LOW) PU/PD decided by SW1.7 TRIGGER_SW ON: 1KΩ PU TRIGGER_SW OFF: 32KΩ PD (min)	Proprietary

Table 9: SOM-352 mini PCIe row 1 pinout

Pin	Symbol	Type	Level (V)	Description	Note
2	3.3 Vaux	P	3.3	Powered by 5V: 115mA (max) Powered by 3.3 Vaux: 3000mA (max)	
4	GND	G	-	Ground	
6	NC	-	-	Not connected	
8	NC	-	-	Not connected	
10	NC	-	-	Not connected	
12	NC	-	-	Not connected	
14	NC	-	-	Not connected	
16	NC	-	-	Not connected	
-	KEY	-	-	Mechanical key	
18	GND	G	-	Ground	
20	NC	-	-	Not connected	
22	PERST#	I (PU)	3.3	CRATON2 reset (2KΩ PU, active LOW) Signal rising edge (0 → 1) will reset mPCIe module	
24	3.3 Vaux	P	3.3	Powered by 5V: 115mA (max) Powered by 3.3 Vaux: 3000mA (max)	
26	GND	G	-	Ground	
28	NC	-	-	Not connected	
30	NC	-	-	Not connected	
32	NC	-	-	Not connected	
34	GND	G	-	Ground	
36	USB_D-	I/O	0.4	USB data line -	
38	USB_D+	I/O	0.4	USB data line +	
40	GND	G	-	Ground	
42	NC	-	-	Not connected	
44	NC	-	-	Not connected	
46	BOOTSTRP	I (PD)	3.3	BOOT_SW ON: 0 or NC: Boot from NAND 1: Boot from USB0 (DFU mode) BOOT_SW OFF: 0/1/NC: Boot from USB0 (DFU mode)	Proprietary
48	NC	-	-	Not connected	
50	GND	G	-	Ground	

Pin	Symbol	Type	Level (V)	Description	Note
52	3.3 Vaux	P	3.3	Powered by 5V: 115mA (max) Powered by 3.3 Vaux: 3000mA (max)	

7.3. I/O Cable Pinout

The I/O cable can help user to install SOM-352 on an existing mPCIe system board without modifying the system board hardware.

Please note that the pinout listed here is seen from the SOM-352 side. For designing an I/O cable interface on the system board, the input and output direction must be reversed.

Table 10: I/O cable pinout

Pin	Name	Type	Level (V)	Description
J1.1	5V	P	5	5V power, OR'ing with 3.3V single voltage mode
J1.2	RXD	I	3.3	UART RXD (PU) Internally tied with mPCIe P17
J1.3	TXD	O	3.3	UART TXD (PU) Internally tied with mPCIe P19
J1.4	EX_RSTn	I	3.3	CRATON2 reset (PU) Internally tied with mPCIe P22
J1.5	1PPS	I	3.3	1PPS (PU) Internally tied with mPCIe P49
J1.6	TAMPER#	I	3.3	Active LOW Internally tied with mPCIe P51
J1.7	GND	G	-	Ground

The 7-pin cable connector is Molex Pico-Lock system **504051-0701** and the contact is **504052-0098**.

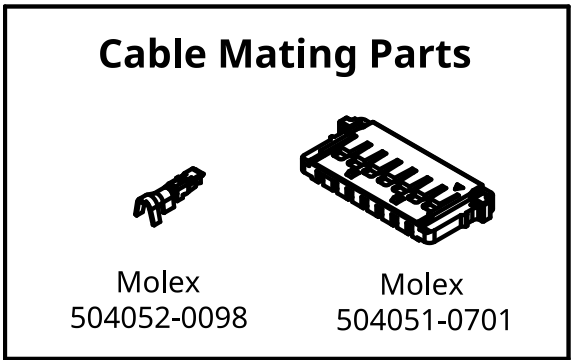

Figure 6: I/O Cable mating component P/N

7.4. DIP Switch

The onboard DIP switch can help user to direct power and I/O signals from either mPCIe interface or the I/O cable. The tamper signal trigger mode and firmware upgrade can also be selected by user.

Figure 7: Onboard DIP switch

Please note that the in SW1.1 to SW1.6, the OFF position actually disconnects the power/signal from the mPCIe pin, while the ON position ties mPCIe pins and I/O cable pins together. In order to avoid interference and to keep 5V power from damaging your system board, it is important to set the DIP switch to correct positions before connecting the I/O cable.

Switching of internal/external GNSS and 1PPS signal is not controlled by DIP switch. Please see 8.8 1PPS for detailed instruction.

Table 11: DIP Switch Functions

Position	Name	ON Function	OFF Function
SW1.1	5V_SW	5V power from mPCIe	5V power from cable, or 3.3V single voltage mode
SW1.2	RXD_SW	UART RXD from mPCIe	UART RXD from cable
SW1.3	TXD_SW	UART TXD from mPCIe	UART TXD from cable
SW1.4	EX_RSTn_SW	CRATON2 reset from mPCIe	CRATON2 reset from cable
SW1.5	1PPS_SW	External 1PPS from mPCIe	External 1PPS from cable
SW1.6	TAMPER#_SW	TAMPER# from mPCIe	TAMPER# from cable
SW1.7	TRIGGER_SW	Trigger when tamper SW close to ground (1KΩ PU)	Trigger with tamper SW open from 3.3V (32KΩ PD)
SW1.8	BOOT_SW	Boot from NAND	Boot from USB0 (DFU)

8. Design-in Guidelines

The SOM-352 pinout is compatible with most standard PCIe mini card interfaces. However, it may need to be fed with 5V DC power and connecting other I/O interfaces through an external cable when installed on an existing mPCIe system board. A customized PCIe mini card pinout can help user to get rid of the extra cable and to rely on the PCIe mini card interface alone. A design-in system board solution may provide improved reliability, simpler installation, and cost saving to the overall system.

8.1. Power Line Traces

- Power line traces should be as wide as possible, in order to reduce impedance of these lines.
- Crossing by any other lines of upper or lower layer should also be avoided.
- The maximum power consumption occurs during RF transmission. A typical transmitting frame lasts 1-2ms.
- It is recommended to keep the 5V supply current no less than 2A (continuous) to keep RF performance from degradation.
- If the SOM-352 halts or resets while performing a V2X RF transmission, it is recommended to add a bulk capacitor on the 5V trace near the mPCIe connector to

lower the impedance of the 5V power rail.

8.2. Power Sequence

- 5V should be supplied prior to 3.3 Vaux.
- If 3.3 Vaux is fed before 5V, user should toggle the EX_RSTn signal after 5V is supplied.
- If it is intended to save power when the SOM-352 is not in use, it is suggested to pull low the EX_RSTn/PERST# pin instead of cutting off 5V power. Once the EX_RSTn/PERST# pin is pulled low, the SOM-352 will enter standby mode, and the power consumption will reduce to 10mA in about 10 seconds.

8.3. Brown Out

- If the 5V power supply drops below 3.5V, the SOM-352 will enter standby mode.
- A SOM in standby mode will stay in this mode until reset.
- Once the power supply returns to normal, the SOM-352 can reboot into normal operation with the rising edge of PERST# or EX_RSTn signal.

8.4. Grounding

- Ensure good GND connection between the ground of the module and the ground of the system board.
- Grounding of the external components (e.g., capacitors) should be connected to the same reference ground of the module and not just on the top layer, use more than one via whenever possible to ensure good GND connection.

8.5. USB Data Lines

The SOM-352 mPCIe module includes a Universal Serial Bus (USB) transceiver, which operates at USB high-speed (480 Mbits/s). It is compliant with the USB 2.0 specification and can be used for control and data transfers as well as for diagnostic monitoring and firmware upgrade.

The USB port is typically the main interface between the SOM-352 mPCIe module and OEM hardware. Since the USB_D+ and USB_D- signals have a clock rate of 240 MHz, the signal traces must be routed carefully. Minimize trace lengths, number of vias, and capacitive loading.

The layout guidelines for the USB data lines (mPCIe pin 36, 38) is listed below. And a

routing example for two pairs of USB data buses is shown in FIGURE 8: USB DATA LINE ROUTING EXAMPLE.

- The impedance value should be as close as possible to 90 Ohms differential.
- The differential pair signals should be all referenced to ground.
- Differential pair route in parallel and in equal length.
- The amount of vias and corners used for the USB signal layout should be minimized; this is to prevent the occurrence of reflection and impedance changes.
- Each pair of USB data lines is required to be parallel to each other with the same trace length, and not parallel with other signals to minimize crosstalk.
- Separate the signal traces into similar groups and route similar signal traces together. In addition, it is recommended to have differential pairs routed together on the system board.
- For the USB traces, do not route them under oscillators, crystals, clock synthesizers, magnetic devices or IC's which could be using duplicate clocks.

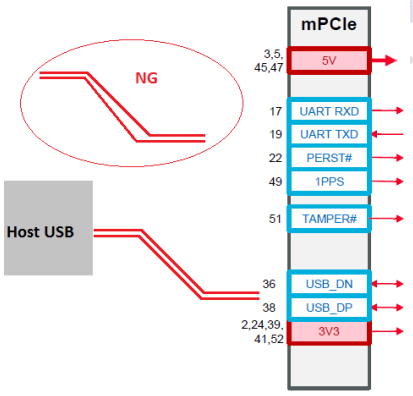

Figure 8: USB data line routing example

8.6. Serial Port

The serial port is typically a secondary interface between the SOM-352 mPCIe module and OEM hardware. The levels for SOM-352 UART is 3.3V TTL logic level.

Depending on the design of serial port on the OEM hardware, a level translator circuit might be needed to make the system operate properly (e.g., 5V to 3.3V or 1.8V to 3.3V). The only configuration that does not need level translation is the 3.3V UART.

8.7. Reset

The reset pin (PERST#, P22) is low active, and will reboot Linux when a rising edge of input voltage (end of assertion) is detected. The reset pin is internally connected to 3.3V with a 2KΩ pull-up resistor. Connecting this pin to an open drain or open collector driver is recommended if the motherboard logic level is different from 3.3V TTL.

8.8. 1PPS

The 1PPS pin (P49) serves as the input of an external 1PPS (1 pulse per second) signal. The start of a system time (UTC time) second will line up with the rising edge of this time pulse signal. For timing and logic level of external 1PPS signal, please see TABLE 2. RECOMMENDED OPERATING CONDITIONS. Leave this pin open if not used.

External 1PPS pins are exposed in both mPCIe interface pin 49 and I/O cable pin 5. To avoid back powering and latch-up, external 1PPS should be fed to SOM-352 at least 20ms later than SOM-352 power up.

The 1PPS input pins (mPCIe pin 49 and I/O cable pin 5) will be pulled high by default during boot-up (up to 200ms). If the 1PPS also serves as BOOT MODE pin in the external GNSS module, for example like some Teseo III modules, it may cause boot-up failure of the external GNSS module. If this happens, you may need choose one of the following three solutions:

1 Add a 3KΩ PD resistor on the motherboard side. (The internal PU resistance of SOM-352 is 32KΩ-60KΩ Ohm)
2 Delay the boot-up of external GNSS module for 200ms until SOM-352 boot-up completed.
3 Pull low the PERST#/EX_RSTn signal during power up, and then release (or pull high) the PERST#/EX_RSTn after the external GNSS module boot-up complete. The 1PPS pin (P49) will remain LOW until the release of PERST#/EX_RSTn signal.

By default, the SOM-352 will use internal 1PPS signal. In order to change to external 1PPS and NMEA source, please issue the following commands in user space:

```
echo 100 > /sys/class/gpio/export
echo out > /sys/class/gpio/gpio100/direction
echo 0 > /sys/class/gpio/gpio100/value          # 0=Ext_GNSS, 1=Int_GNSS
```

To let the above setting take effect upon next boot-up, please append the above lines in `/home/root/ext-fs/usr/bin/at_startup`.

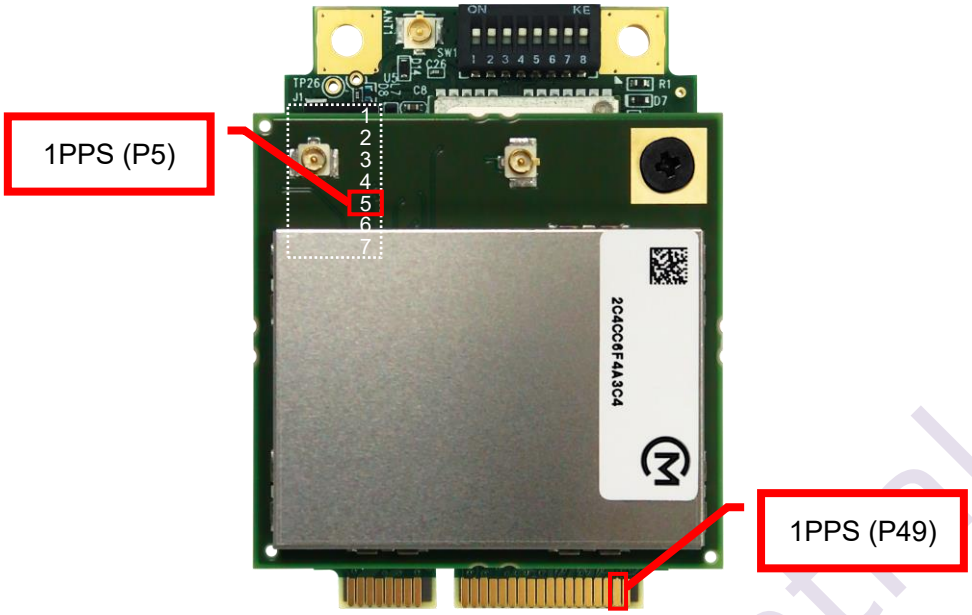

Figure 9: External 1PPS input pins

8.9. BOOTSTRP

The BOOTSTRP pin (P46) will be sampled during the first 10ms upon power up. If the BOOTSTRP is pulled HIGH (3.3V), the SOM-352 system will enter DFU (Device Firmware Upgrade) mode and allows the host system to flash the entire NAND via USB0 at once; otherwise, it will boot normally from NAND.

It is recommended to use a 0 Ohm resistor to pull-up the BOOTSTRP pin. The pull-up resistor of BOOTSTRP should not exceed 5 KOhm.

8.10. Tamper Detection (Optional)

The tamper detection function will be supported by project base. It is disabled by default.

The SOM-352 has to be powered up for the tamper detection function to work. The design and implementation of a backup power source is not in the product scope and should be considered by the user.

The tamper detection mechanism is part of the FIPS 140-2 Level 3 security requirements. The tamper detection itself is carried out entirely in HW. On SW level, there is only an API that allows enabling the tamper detection mechanism. Calling this API will move tamper HW state from the testing mode to the production mode. Once called, it

cannot move back to the testing mode.

The source and trigger mode of tamper detection signal can be selected with the DIP switch on SOM-352, position SW1.6 and SW1.7.

Tamper detection pins are exposed in both mPCIe interface pin 51 and I/O cable pin 6. Pulling the tamper detection pin to ground will trigger a tamper event, indicating that the enclosure of the system has been opened without proper authorization. User can enable one of the two tamper modes in API:

1 Production mode
2 Test mode.

8.10.1. Production Mode

In production mode, the SOM-352 will erase the CSP (critical security parameter) material saved in eHSM. The eHSM hardware will be left unusable because the CSP cannot be rewritten to the chip anymore. Two additional tamper modes are available when entering production mode: normal mode and standby mode.

8.10.1.1. Normal Mode

Tamper response provides protection against tamper attempts during operational state when the chip is powered on. When it is enabled, tamper event will immediately trigger the zeroization sequence. Enabling this mode is done by invoking the Enable Normal mode tamper response service API.

8.10.1.2. Standby Mode

Tamper response provides protection against tamper attempts while the chip is in sleep mode state. When it is enabled, any previously latched tamper event during sleep mode will trigger the zeroization sequence upon power-up. Enabling this mode is done by invoking the Enable standby mode tamper response service API.

8.10.2. Test Mode

In test mode, the SOM-352 will not erase the CSP (critical security parameter) material saved in eHSM. Each invocation of the tamper signal increments an internal counter within the eHSM. This counter can then be inquired by calling the eHSM runtime status API,

providing evidence for the tamper signal detection.

8.11. Thermal Management

If performing heavy V2X transmission on SOM-352, it is recommended to add thermal vias and expose bare copper top layer on the system board to help disperse heat. Inserting a soft silicone thermally conductive pad between the system board and SOM-352 could facilitate heat dispersion to the system board more efficiently.

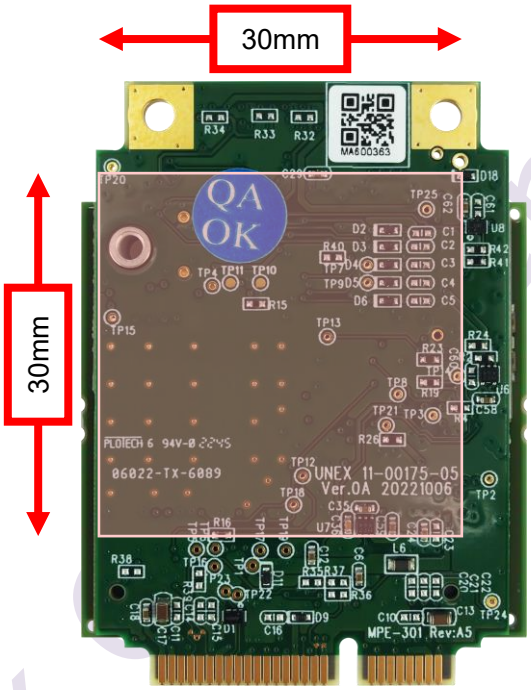

Figure 10: Thermally conductive pad area

8.12. Firmware Upgrade

8.12.1. Manual control

When the mPCIe Pin 46 (BOOTSTRP) is left unconnected (floating) or connected to ground, the BOOT_SW (SW1.8) controls the boot mode. See TABLE 11: DIP SWITCH FUNCTIONS for more details.

- BOOT_SW ON: Normal boot (boot from NAND)
- BOOT_SW OFF: Firmware upgrade (boot from USB0, DFU mode)

8.12.2. Host GPIO control

When the mPCIe Pin 46 (BOOTSTRP) connects to a host system GPIO, and the BOOTSW (SW1.8) is kept at ON position, the host system GPIO controls the boot mode. See TABLE 9: SOM-352 MINI PCIE ROW 1 PINOUT for more details.

- BOOTSTRP LO: Normal boot (boot from NAND)
- BOOTSTRP HI: Firmware upgrade (boot from USB0, DFU mode)

9. Dimensions and Weight

The SOM-352 module follows the PCIe full-mini card form factor, but 8.5mm wider than the standard 30mm width. When designing a system board, at least 3mm clearance on both left and right side is needed to avoid component interference. It is also recommended to reserve 13mm as total height limitation. Please refer to *PCI Express Mini Card Electromechanical Specification 2.0/2.1* for more detailed guidelines.

It is recommended to use a mini PCIe connector with 4mm stack height, leaving 1.5mm space between the SOM-352 PCB and the system board. This space can later be filled with silicone thermal conductive pad to help dissipate the heat generated by SOM-352 to the system board PCB. User can choose *TE 2041119-1* as a candidate for such a mini PCIe connector.

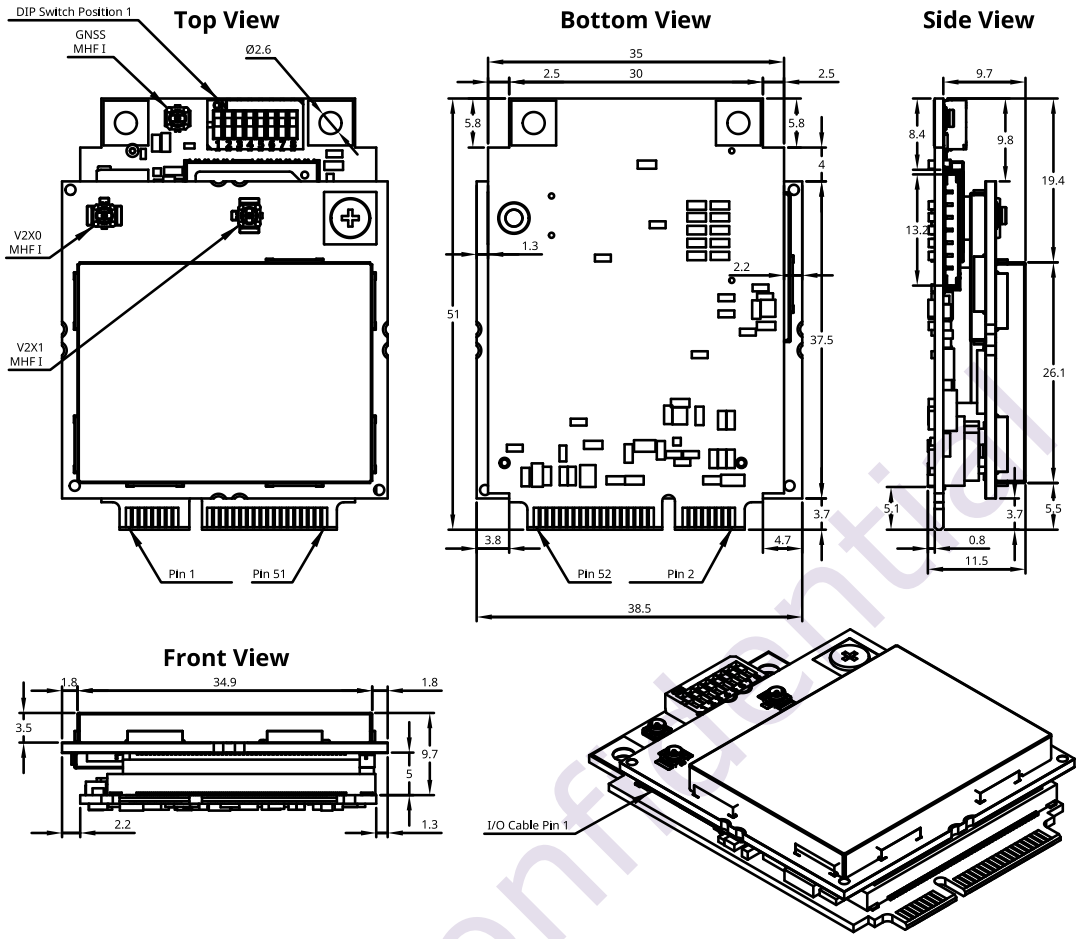

Figure 11: SOM-352 dimensions

Table 12: Dimensions and weight

Model	Length (mm)	Width (mm)	Height (mm)	Weight (g)
SOM-352	51.0	38.5	11.5	21.2

9.1. Component Keep Out Area

Maximum height of bottom side components may reach 1.0mm. In order to avoid interference with SOM-352, the system board side component height should be carefully considered according to the datasheet of mPCIe connector selected.

10. Software Settings

The following BSP settings are applicable for Unex software package only.

Table 13: Unex BSP interface settings

Function	Description
Console	UART3, 115200bps, 8N1, ttyAMA2
GNSS NMEA	UART1, 230400bps, 8N1, ttyAMA1
GNSS Debug (Opt.)	UART2, 230400bps, 8N1, ttyAMA0
GNSS Reset	GPIO111, 0->1 = GNSS module reset (cold start, clear SRAM and RTC)
Ext GNSS SW	GPIO100. 0=Ext_GNSS, 1=Int_GNSS (default=1)
S_GPIO3	GPIO99, functioning as PPS1
1PPS	GPIO29 (main), GPIO25 (aux)
USB0	Default USB 2.0 device mode. RNDIS device IP = 192.168.1.3, RNDIS host IP = 192.168.1.1
V2X0 antenna detection	/sys/bus/iio/devices/iio\:device0/in_voltage4_raw
V2X1 antenna detection	/sys/bus/iio/devices/iio\:device0/in_voltage5_raw
MAC address	grep V2X_0 /etc/unex/device/device_info.txt
BSP/protocol version	/etc/unex/update.log

10.1. Verifying the Integration with a Host System

The following descriptions are applicable for Unex software package only.

10.1.1. Windows 10/11

For verifying the integration of a SOM-352 with a Windows host system, please follow the steps below:

1 Install SOM-352 into a mini PCIe slot on a Windows host computer.

2 Check if a network adapter named “**Remote NDIS Compatible Device**” can be found in Device Manager.

3 Open Command Prompt on the Windows host.

4 Ping the RNDIS device IP of SOM-352 and check if it is alive.

```
C:\Users\user> ping 192.168.1.3
```

5 Open a SSH terminal to SOM-352 and check if it works.

```
C:\Users\user> ssh-keygen -R 192.168.1.3 & ssh root@192.168.1.3
```

For most Windows 10/11 systems, the RNDIS host driver is installed by default. The Windows host will assign a default IP `192.168.1.1` to this new RNDIS network adapter. This default host IP address is configured in `/etc/network/udhcpd.conf` on the SOM-352 filesystem and can be modified if needed.

10.1.2. Linux

For verifying the integration of a SOM-352 with a Linux host system, please follow the steps below:

1 Install SOM-352 into a mini PCIe slot on a Linux host computer.

2 Open terminal on the Linux host.

3 Check if the RNDIS driver has already been installed on the host system. If it has not been installed yet, install the RNDIS driver for the host system. The driver installation might include loading `rndis_host.ko` with `modprobe` command or enabling `CONFIG_USB_NET_RNDIS_HOST` when compiling the Linux kernel. The detailed instructions of installing the RNDIS driver are not included here because it may vary from one distribution to another.

```
user@host:~$ lsmod | grep rndis
```

4 Check if the Unex device has been registered as a RNDIS device with a network interface.

```
user@host:~$ dmesg | grep -i -C4 unex
```

5 Ping the RNDIS device IP of SOM-352 and check if it is alive.

```
user@host:~$ ping 192.168.1.3
```

6 Open a SSH terminal to SOM-352 and check if it works.

```
user@host:~$ ssh-keygen -R 192.168.1.3 ; ssh root@192.168.1.3
```

11. Troubleshooting

11.1. Repetitive Resetting When Using 3.3V Single Voltage Supply

Although a SOM-300 family module is capable of using 3.3V single voltage supply, the stability is still largely dependent on the actual design of the motherboard 3.3V rail. If the 3.3.V rail impedance is not low enough, the transient current drain during RF transmission will cause a voltage dip, and hence triggering a system reset.

If repetitive resetting happens when mounting on an off-the-shelf 3.3V mPCIe slot, please consider supplying 5V power from J1.1 instead.

11.2. No Response After Applying Power

This phenomenon may come from multiple causes. Please follow the steps below to check each one of them:

1 Check if the 5V/3.3V power have been properly supplied by your motherboard.
2 Check if the SW1.1 setting matches your hardware configuration.
3 Check if the SW1.8 setting is at ON (Boot from NAND) position.
4 Connect the UART console to your host.
  4.1 If you have a design-in UART interface in mPCIe P17/P19, make sure to keep the SW1.2/SW1.3 at ON position.
  4.2 If you do not have design-in UART, please connect the I/O cable for UART interface and keep the SW1.2/SW1.3 at OFF position.
5 Check if the RNDIS driver has been properly installed on your host system.
6 Check if the IP address 192.168.1.1 has been assigned to another network interface other than the RNDIS interface. If it has already been assigned, it is required to perform either of the following operations:
  6.1 Change the IP setting of that network interface and leave 192.168.1.1 available for the SOM-300 family RNDIS interface.
  6.2 Change the SOM-300 family RNDIS IP address setting. Please refer to the CHANGING SYSTEM IP ADDRESS section in Unex's documentation, which can be found in Unex's software release package.